AMENDMENTS TO THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line 2, with the following rewritten paragraph:

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which like reference numbers indicate like features and wherein:

Figures 1A and 1B illustrate ~~Figure 1 illustrates~~ the scan testing circuit design for a SoC in accordance with the present invention;

Figures 2 displays the clock control mechanism implemented in the scan testing circuit design of Figure1;

Figures 3 shows the scan enable registering logic of Figure1;

Figure 4 illustrates the clock generator for scan chain group A of Figure 1;

Figure 5 shows the clock generator for scan chain group B of Figure 1;

Figure 6 displays the clock generator for scan chain group C of Figure 1;

Figure 7 illustrates the test mode select arrangement for the test mode delta signal TMΔ of Figure 2;

Figure 8 illustrates the test mode select arrangement for the simultaneous test mode signal TM_{ALL} and intermediate control signals, sig_A, sig_B, and sig_C ~~of Figure 2~~; and

Figure 9 displays the test mode select arrangement for the first, second and third test mode signals, TM_1, TM_2, and TM_3, and the VLCT mode signal $VLCT_M$ of Figure 2.

Please replace the paragraph beginning at page 8, line 23, with the following rewritten paragraph:

Figure 1A ~~1~~ illustrates the scan test circuit design for a mixed signal SoC in accordance with the present invention. For simplicity, Figure 1A ~~1~~ clearly

shows three of the four groups, A, B, C, and D. The three scan chain groups, A, B, and C, as illustrated, couple between respective scan input and output terminals. Specifically, scan chain group A couples between input terminal $Input_1$ and output terminal $Output_1$. Scan chain B couples between input terminal $Input_2$ and output terminal $Output_2$ and scan chain C couples between input terminal $Input_3$ and output terminal $Output_3$. Each scan chain group A, B, and C include a demultiplexer unit, a first multiplexer unit, a scan chain, and a second multiplexer unit. Scan chain group A, in particular, includes demultiplexer unit 102, first multiplexer unit 110, scan chain 118 and second multiplexer unit 126. Demultiplexer unit 102 couples to receive test stimulus through input terminal $Input_1$. It demultiplexes the test stimulus to provide function inputs and the test stimulus along with the first multiplexer unit 110. A testing clock signal TEST provides the clocking for demultiplexer unit 102. A controlling demultiplexer 108 also couples to first multiplexer unit 110 to provide the appropriate control for testing scan chain group A. Controlling demultiplexer 108 couples to demultiplexer 106 and couples to receive signals TM_1, TM_2, TM_3, and TM_{ALL}. TM_1 represents a shift scan instruction to shift all Group A scan chains. Accordingly, TM_2 represents a shift scan instruction to shift all Group B scan chains and TM_3 represents a shift scan instruction to shift all Group C scan chains. TM_{ALL} represents that a capture scan instruction is issued to capture on all scan chain groups. First multiplexer unit 110 provides a multiplexed signal to scan chain 118, wherein the scan chain is comprised of at least one flip-flop controlled by a clock control mechanism 116, as shown in Figure 1B. Clock control mechanism 116 couples to receive test mode select pins [n:0], a scan enable signal $SCAN_{EN}$, a test clock signal $TEST_{CLK}$ and the functional enable and clocking signals, F_{EN}_A, F_{EN}_B, F_{EN}_C, F_{CLK}_A, F_{CLK}_B, F_{CLK}_C, for each of the scan chain groups, A, B, and C, respectively. The clock control mechanism 116 derives a control signal CLK_A, CLK_B, and CLK_C for each scan chain group A, B, and C, respectively to concurrently clock in the test stimulus input data into each scan chain at its predetermined frequency. A controlling multiplexer 124 couples to receive the output of scan chain 118. Multiplexer 124 is used when a scan is

performed on VLCT. The multiplexer routes the scan output of groups A, B, or C according to the respective test mode TM_1, TM_1, or TM_2. In a non-VLCT mode, where all the scan groups can be exercised in parallel, the respective output multiplexers are used. In addition, scan chain 118 connects to second multiplexer 126 to provide the resultant data. The functional output represents resultant data when the SoC has performed correctly given the same test stimulus. This functional output is transmitted to the second multiplexer 126. Accordingly, the second multiplexer 126 provides a multiplexed output between the two results as input for determining whether there is an error or not. As stipulated earlier scan chain group B, and C include respective demultiplexer units, 104 and 106, first multiplexer units, 112 and 114, scan chains, 120 and 122, and second multiplexer units, 128 and 130. Scan chain groups B and C have similar arrangements to that of scan chain group A. Notably, there may be more than three scan chain groups.

Please replace the paragraph beginning at page 14, line 14, with the following rewritten paragraph:

Figure 3 illustrates the schematic for scan logic 202 of Figure 2 which generates enable signals, EN_{RISE} and EN_{BOTH}. As shown, DQ flip-flop 302 receives the scan enable signal $SCAN_{EN}$ and the test clock signal $TEST_{CLK}$. The output of flip-flop 302 is inverted by inverter 304 to provide input for AND gate 306. AND gate 306 also couples to receive the scan enable signal $SCAN_{EN}$ to provide at its output the enable signal EN_{RISE}. Enable signal EN_{RISE} detects a rising edge on the scan enable (chip input), scan enable signal $SCAN_{EN}$. XOR ~~NOR~~ gate 308 couples to receive the scan enable signal $SCAN_{EN}$ and the output of flip-flop 302 to provide at its output the enable signal EN_{BOTH}. Enable signal EN_{BOTH} detects a rising or falling transition on scan enable input. These two signals, EN_{RISE} and EN_{BOTH}, are used for gating off the clock pulse whenever there is a transition on scan enable $SCAN_{EN}$. For scan testing on a high end

tester, the clock pulse must be gated off whenever a capture has been performed and a shift is to follow. For example, in the case when the scan enable transitions from "0" to "1". This is necessary as one clock pulse is needed for the transition on the scan enable input $SCAN_{EN}$ to be registered internally. For scan testing on the VLCT platform, in addition to above clock gating, the clock pulse must also be gated off when the test mode changes, i.e., when the test mode select pins are changed to shift a different scan group.

Please replace the paragraph beginning at page 15, line 1, with the following rewritten paragraph:

Figure 4 shows how the signals are used to gate the clock for the scan chain group A. Although this figure illustrates Group A alone, Figures 5 and 6 demonstrate that the gating for the other groups, B and C, and are identical. More particularly, Figure 4 illustrates the clock generator 206 for scan chain group A of Figure 2. Inverters, 408 and 410, couple to receive the VLCT mode signal $VLCT_M$ and the enable signal EN_{RISE}, respectively. The signal $VLCT_M$ is a decoded output of the test mode select inputs and indicates a VLCT test mode. AND gate 412 connects to inverters, 408 and 410 and provides input to OR gate 414. OR gate 402 couples to receive the enable signal EN_{BOTH} and the test mode delta signal TMΔ. Inverter 404 inverts the output of OR gate 402 to be provided as input to AND gate 406. AND gate 406 connects to receive the first test mode signal TM_1. First test mode signal TM_1 is again a decoded output of the test mode select inputs [n:0] that indicates that scan chain group A is being shifted. OR gate 414 connects to AND gates, 406 and 412 to generate group A enable signal EN_A. When the VLCT mode signal $VLCT_M$ is "0," the scan test circuitry is in a non-VLCT test mode. The enable signal EN_{RISE} is used for clock gating. When this signal is high, the scan test circuitry is in a VLCT mode. Both the enable signal EN_{BOTH} and the test mode delta signal TMΔ are used to gate off the clock pulse. The enable signal EN_A is generated and used to gate the clocks through clock-gating macros, 417 and 423, as shown. DQ flip-flop 416 couples

to receive enable signal EN_A at its D input. Inverter 418 inverts the test clock signal $TEST_{CLK}$ for the enable input of flip-flop 416. AND gate 420 connects to the output of flip-flop 416 and receives the test clock signal $TEST_{CLK}$. XOR ~~NOR~~ gate 422 couples to AND gate 420 and receive a polarity clock signal $TCLK_P$. Polarity clock signal $TCLK_P$ provides additional gating. It comes from a programmable test register that is used to invert the clock if required. The D input of DQ flip-flop 426 connects to the output of XOR ~~NOR~~ gate 422. Inverter 424 inverts the functional clock F_{CLK}_A for the enable input of flip-flop 426. AND gate 428 connects to the output of flip-flop 426 and receives the functional clock F_{CLK}_A. Finally, the test clock is multiplexed with the functional enable signal F_{EN}_A using clock gating macro 423. As shown, multiplexer 430 connects to AND gate 428 and receives the functional enable signal F_{EN}_A to generate clock signal CLK_A, wherein test mode signal TM provides the control for multiplexer 430.

Please replace the paragraph beginning at page 16, line 3, with the following rewritten paragraph:

Figure 5 illustrates the clock generator 208 for scan chain group B of Figure 2. Inverters, 508 and 510, couple to receive the VLCT mode signal $VLCT_M$ and the enable signal EN_{RISE}, respectively. AND gate 512 connects to inverters, 508 and 510 and provides input to OR gate 514. OR gate 502 couples to receive the enable signal EN_{BOTH} and the test mode delta signal TMΔ. Inverter 504 inverts the output of OR gate 502 to be provided as input to AND gate 506. AND gate 506 connects to receive the second test mode signal TM_2. OR gate 514 connects to AND gates, 506 and 512 to generate group B enable signal EN_B. DQ flip-flop 516 couples to receive enable signal EN_B at its D input. Inverter 518 inverts the test clock signal $TEST_{CLK}$ for the enable input of flip-flop 516. AND gate 520 connects to the output of flip-flop 516 and receives the test clock signal $TEST_{CLK}$. XOR ~~NOR~~ gate 522 couples to AND gate 520 and receive a polarity clock signal $TCLK_P$. The D input of DQ flip-flop 526 connects to the output of

XOR ~~NOR~~ 522. Inverter 524 inverts the functional clock F_{CLK}_B for the enable input of flip-flop 526. AND gate 528 connects to the output of flip-flop 526 and receives the functional clock F_{CLK}_B. Multiplexer 530 connects to AND gate 528 and receives the functional enable signal F_{EN}_B to generate clock signal CLK_B. Test mode signal TM provides the control for multiplexer 530.

Please replace the paragraph beginning at page 16, line 20, with the following rewritten paragraph:

Figure 6 illustrates the clock generator 210 for scan chain group C of Figure 2. Inverters, 608 and 610, couple to receive the VLCT mode signal $VLCT_M$ and the enable signal EN_{RISE}, respectively. AND gate 612 connects to inverters, 608 and 610 and provides input to OR gate 614. OR gate 602 couples to receive the enable signal EN_{BOTH} and the test mode delta signal TMΔ. Inverter 604 inverts the output of OR gate 602 to be provided as input to AND gate 606. AND gate 606 connects to receive the third test mode signal TM_3. OR gate 614 connects to AND gates, 606 and 612 to generate group C enable signal EN_C. DQ flip-flop 616 couples to receive enable signal EN_C at its D input. Inverter 618 inverts the test clock signal $TEST_{CLK}$ for the enable input of flip-flop 616. AND gate 620 connects to the output of flip-flop 616 and receives the test clock signal $TEST_{CLK}$. XOR ~~NOR~~ gate 622 couples to AND gate 620 and receive a polarity clock signal $TCLK_P$. The D input of DQ flip-flop 626 connects to the output of XOR ~~NOR~~ gate 622. Inverter 624 inverts the functional clock F_{CLK}_C for the enable input of flip-flop 626. AND gate 628 connects to the output of flip-flop 626 and receives the functional clock F_{CLK}_C. Multiplexer 630 connects to AND gate 628 and receives the functional enable signal F_{EN}_C to generate clock signal CLK_C. Test mode signal TM provides the control for multiplexer 630.

Please replace the paragraph beginning at page 17, line 6, with the following rewritten paragraph:

Figures 7, 8 and 9 display the test mode select signal decode logic 204 of Figure 2. Figure 7 shows the generation of the test mode delta signal TMΔ which indicates when the test mode has changed. This signal indicates to the clock gating logic of Figures 4, 5, and 6 that a different group is now being shifted. Specifically, Figure 7 includes flip-flops, 702, 704, 706 and 708, coupled to receive the signals from the test mode select pins [n:0] and the test clocking signal $TEST_{CLK}$. XOR ~~NOR~~ gates, 710, 712, 714, and 716, couple respectively to the D inputs and outputs of flip-flops, 702, 704, 706 and 708, respectively. OR gate 718 connects to the outputs of XOR ~~NOR~~ gates, 710, 712, 714, and 716 to generate the test mode delta signal TMΔ.